ADAS: A Safe Eye on The Road

FTF-AUT-F0334

Yolanda XI | BD Manager

MAY. 2014
Mobility: Independence, Freedom and Fun

From independent Drivers to Autonomous Cars
Evolution of Advanced Driver Assistance Systems

Collision Mitigation
Passive Systems

Collision Avoidance
Reactive Systems

Collision Prediction
Predictive and Warning

Semi-Autonomous
Predictive Actuators
A simplified Taxonomy for ADAS

**Today**
- Sensor
- Driver active
- Fail Safe

**Automate**
- Sensor Fusion & maps
- Co-Pilot
- Dependable & reliable

**By 2020**
- Sensors & Maps & V2X
- Driverless
- Fail operational

**Autonomous**
- Commercial autonomous vehicles (drones-big vehicle)
- Driverless public transport
- ACC with Steer

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- ACC
- LDW
- BSD
- Head Light
- TSR
- Park Assist
- EBA
- Highway platoons
- ACC with Steer
Automated Vehicle Model

- **Driver Fatigue**
  - Drowsiness camera
  - Steering trend

- **Driving Style**
  - RPM, Gas pedal Monitoring,…

- **Driver Attention**
  - Eye FoV camera
  - TSR, LDW etc

- **360° & Driver Model**

- **3D Context**
  - Surround See and Sense

- **Steer & Brake**

- **Auto Navigation & Risk assessor**

- **Vehicle Motion**

- **HMI**
Automated Vehicle: disciplines links & relations

- Open Platforms
- Dependable Safety
- Internet of Things
- Vehicle Networking
- Cloud computing
- Big Data
- Security

Automated Vehicles
Self-Driving Platform – Open and Flexible

Sensor Fusion Platform

“Image” Signal Processing

Digital Signal Processing

App Spec Computing (ICP, CV, Radar, GPS)

Sensor Raw Data Distribution & Handling

Feature Detection & Taxonomy

Graphic Processing Unit

Computing Processing Unit

Tracking 3D Model

Data Fusion & Risk Assessment

HMI Self-Action

Sensor Fusion Platform

“Image” Signal Processing

Digital Signal Processing

App Spec Computing (ICP, CV, Radar, GPS)

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Graphic Processing Unit

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Tracking 3D Model

Data Fusion & Risk Assessment

HMI Self-Action

Sensor Fusion Platform
Leveraging an Open Standards Framework

Ecosystem to deliver a safe, secure and open architecture supported by standards
ISO26262 Fault Prevention and Control Measures

... implemented as **product features**
against random faults (architecture, function)

- Triple voted flip flops
- ECC on memories
- Radiation ‘hard’ flip flops
- Redundant vias
- Ultra low alpha mould compound to reduce effect of radiation

... to **prevent faults**
(robustness)

- ISO Design Process
- Proven Technology
- Design Margin
- Process Margin
- Automotive Process Package

... to **control faults**
(detect and react)

- Independent compute engines – 2 x MP2 cluster
- Independent checker engine – Safe State engine
- EDC on memory and buses
- Logic BIST/Memory BIST
- Voltage/temperature monitors

... during **development** and **production**
against systematic faults (process, procedures)

ISO26262 can NOT be retro-fitted !!!
The Market – Freescale & Analyst view

- Market dominated by front view cameras
- Significant growth in smart peripheral view cameras (27% CAGR) and surround view (15% CAGR)

<table>
<thead>
<tr>
<th>Year</th>
<th>Smart Peripheral View Cameras</th>
<th>Peripheral View Cameras</th>
<th>Surround View Systems</th>
<th>Data Fusion Systems</th>
<th>Front View Cameras</th>
</tr>
</thead>
<tbody>
<tr>
<td>2016</td>
<td>$100,000</td>
<td>$200,000</td>
<td>$300,000</td>
<td>$400,000</td>
<td>N/A</td>
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<td>2017</td>
<td>$200,000</td>
<td>$400,000</td>
<td>$600,000</td>
<td>$800,000</td>
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<td>2018</td>
<td>$300,000</td>
<td>$600,000</td>
<td>$900,000</td>
<td>$1,200,000</td>
<td>N/A</td>
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<td>2019</td>
<td>$400,000</td>
<td>$800,000</td>
<td>$1,200,000</td>
<td>$1,600,000</td>
<td>N/A</td>
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<td>2020</td>
<td>$500,000</td>
<td>$1,000,000</td>
<td>$1,600,000</td>
<td>$2,000,000</td>
<td>N/A</td>
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<tr>
<td>2021</td>
<td>$600,000</td>
<td>$1,200,000</td>
<td>$2,000,000</td>
<td>$2,400,000</td>
<td>N/A</td>
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<tr>
<td>2022</td>
<td>$700,000</td>
<td>$1,400,000</td>
<td>$2,400,000</td>
<td>$2,800,000</td>
<td>N/A</td>
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<tr>
<td>2023</td>
<td>$800,000</td>
<td>$1,600,000</td>
<td>$2,800,000</td>
<td>$3,200,000</td>
<td>N/A</td>
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</table>

<table>
<thead>
<tr>
<th>Safe Architecture</th>
<th>Front Sensing</th>
<th>Peripheral Sensing</th>
<th>Data Fusion</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ASIL B (min)</td>
<td>ASIL B (min)</td>
<td>ASIL D</td>
</tr>
<tr>
<td></td>
<td>Quad Cores @ ≥800MHz</td>
<td>Quad Cores @ ≥ 800MHz</td>
<td>Quad Cores @ ≥1000MHz + 2nd SOC</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Sensor Proc</th>
<th>Massively Parallel image processor for detection</th>
<th>Massively Parallel image processor for detection</th>
<th>N/A</th>
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</thead>
<tbody>
<tr>
<td>HMI</td>
<td>2D GFx for debug &amp; HMI</td>
<td>3D GFX for HD display</td>
<td>N/A</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Connectivity</th>
<th>PCIe, MIPI-CSI2</th>
<th>PCIe, ENET, MIPI-CSI2</th>
<th>FD-CAN, FlexRay, ENET</th>
</tr>
</thead>
</table>
## Assumed Safety Goals for Target Applications

<table>
<thead>
<tr>
<th>Application / Safety goals</th>
<th>ASIL</th>
<th>Behavior in case of fault</th>
</tr>
</thead>
</table>
| Adaptive headlight control                                                                 | False positive: ASIL B  
False negative: QM                             | Fail-safe  
(Fail-silent or fail-indicate)                        |
| Driver assist functions  
(lane departure warning, blind spot detection, traffic sign recognition, obstacle/pedestrian detection, collision warning). | False positive: ASIL A  
False negative: ASIL A                           |                                                               |
| Mirror Replacement  
(QM (redundant mirrors) / ASIL A (single mirror))                                         |                                           |                                                               |
| Emergency brake  
(obstacle detection and emergency brake request).                                          | False positive: ASIL B / ASIL C  
False negative: QM                               |                                                               |
| Collision avoidance  
(obstacle detection and active steering)                                                      | False positive: ASIL D  
False negative: QM                               |                                                               |
| Lane keeping                                                                                   | False positive: ASIL C  
False negative: ASIL C                           |                                                               |
| (Semi-) Autonomous driving                                                                  | False positive: ASIL D  
False negative: ASIL D  
(graceful degradation: maintain limited operation in case of a fault) | Failure-tolerant system  
(high availability system) |
Freescale Automotive ADAS Innovation

Safe and Secure – Combination of hardware features and intelligent software to provide high ASIL performance. Secure engine to protect boot and communication.

Flexibility – Tools, drivers and middleware that enables a fast, safe and efficient software development path.

Scalability – Multicore architecture, robust network, combined with highly abstracted, programmable intelligent accelerators to enable all major ADAS application integration.
MRD2001 77 GHz and MPC577xK
Industry’s most comprehensive system-level solution for automotive radar systems

Qorivva MPC577xK
- Replaces:
  - 8 ADC
  - 1 DAC
  - 1 FPGA
  - External SRAM
  - General purpose MCU
- Enables:
  - Significant PCB area saving
  - Reduced assembly cost

MRD2001 77 GHz Chipset
- Replaces:
  - Bare Die RF solutions with a RF Chipset based on RCP package technology
  - Discrete Filter Components and Amplifiers
- Enables:
  - Significantly lower assembly cost
  - Lower PCB cost
MRD2001 77GHz Packaged Radar Chipset

The MRD2001 chipset is a scalable radar solution for high end and low end ADAS applications, industrial safety, security, and robotics

Differentiating Points

• Scalable to 4 TX channels and 12 RX channels
• Activate simultaneous Tx channels for electronic beam steering
• Supports fast modulation at 100 MHz / 100 ns
• Integrated baseband filter and VGA saves system bill-of-materials cost
• Local oscillator at 38 GHz to lower the distribution loss and reduce system interference

Key Characteristics

• Low power consumption 2.5 W typical for the complete transceiver chipset
• Differential Tx outputs delivering minimum 10dBm with 5-bit digital power control
• Advanced packaging technology with BGA format
• Integrated bi-phase modulator for advanced correlation coding
• Built-in receive chain test mode when using RaceRunner microprocessor
• Best phase noise performance < -85 dBc/Hz at 100 kHz offset, and -95 dBc/Hz at 1 MHz offset
• Temperature detector on each MRD2001 chip
Radar Single Chip Transceiver – MRD3000

This chip is a 2Tx/4Rx single chip transceiver scalable to 4Tx/8Rx in master/slave mode

Differentiating Points

• Complete single chip radar transceiver with 2Tx and 4Rx channels
• Dual band 77/79GHz for application to SRR, MRR, and LRR applications
• Fully integrated VCOPLL and programmable chirp generator for fast modulation radar systems
• Fast modulation allows improved multi-target tracking, and direct extraction of obstacle range, speed, and angle.

Key characteristics

• Supported frequency bands, 76-77GHz with 1GHz BW, and 77-81GHz with 2GHz BW
• Phase noise < -105 dBc/Hz @ 10MHz offset
• Low Rx NF typically < 14dBm
• Operation in Master/Slave mode for expansion to 4chTx/8chRx
• Tx channel phase rotator with 5-bit control via SPI for digital beam forming
• Power dissipation targeted at <2.5W (1Tx active, 4chRx, 100% duty cycle)
• Integrated A/D converter with MIPI-CSI2, LVDS digital interface supporting up to 20 MSps
• On chip test mode for transmit and receive path integrity test at system level

Typical Application Diagram

Part number
MRD3000

Alpha Samples: Jan 2015
PPAP: June 2016

Product in Feasibility Phase, subject to change or cancellation without notice.
ADAS Communication Links

<table>
<thead>
<tr>
<th>Analog (PAL / NTSC)</th>
<th>LVDS</th>
<th>Ethernet (AVB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>✓ Low cost components, widely available</td>
<td>✓ Very high bandwidth (up to 1 Gbps)</td>
<td>✓ Low cost unshielded twisted pair cable</td>
</tr>
<tr>
<td>× Shielded co-axial cabling required</td>
<td>× Expensive shielding required</td>
<td>× High bandwidth up to 250 Mbps full duplex</td>
</tr>
<tr>
<td>× Low resolution and color deviations</td>
<td>× Costly manufacture of cable harness</td>
<td>✓ Widely adopted, ease of use</td>
</tr>
<tr>
<td>× Accepted only for low-end rear view camera</td>
<td>× EMC and quality issues</td>
<td></td>
</tr>
</tbody>
</table>

*Ethernet is proven alternative to conventional video communication*
Multi-Camera Panorama View Park Assist

**Challenge**
- LVDS based solution requires FPGA for multiplexing
- Separate DSP leads to high BOM cost

**Solution**
- GPU efficiently does video stitching and rendering
- Fully integrated i.MX6 single to quad-core MPU with powerful GPU offers low BOM cost
Salsa 512K – MPC5604E

Core
- up to 64 MHz PowerPC ISA e200 zen0h core

Memory
- 512k byte Program Flash with ECC
- 4x16k byte Data Flash with ECC
- 96k byte SRAM with ECC

I/O
- 1 x MJPEG video encoder with image sensor interface supporting up to 1.2MPixel
- 1 x 10/100 Ethernet MAC incl. IEEE 1588 PTP support
- 1 x FlexCAN
- 2 x LinFlex
- 1 x I2C interface
- 1x I2S/I8S/TDM audio interface
- 2 x DSPI (4 independent chip selects each)
- 1 x eTimer (6 channels for general purpose)
- 1 x ADC (5V capable)
  - TBD Ch, 10-bit, conversion time <1µsec

System
- PLL
- 16Ch eDMA
- 16MHz internal RC OSC
- 2 or 5 pin JTAG / Nexus Class 1
- 3.3V single supply
- 64 pin LQFP package

http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MP
C5604E&nodeId=01624606C1427E
First Production Ethernet Surround Camera System – SOP 2013 (Freescale MPC5604E + Ethernet Camera SW application)
MPC5604EKIT

Complete Camera Dev Platform
- Freescale MPC5604E mini daughter card for video compression and transmission over Ethernet
- Freescale Ethernet camera streaming software (for development purposes only)
- Aptina Image Sensor and ISP daughter card (AP0132+AP0101)
- Broadcom Ethernet PHYs supporting Broadreach and standard 100Mbps (BCM99810 and BCM5241)

MPC5604EKIT simplifies development
- Simplifies sourcing (purchase Kit from one vendor – Freescale)
- Free evaluation Software
- Reduces costs - $150 kit price

MPC5604EKIT Applications
- Automotive Vision & Ethernet Gateways
- Industrial
- Door Entry systems – commercial and residential
- Security cameras - commercial and residential
- White Goods applications – Refrigerators and washing machines
- Avionics – In seat video calls
- Mobile machinery, Elevators

MPC5604EKIT available from June 2014
MPC5606E – Automotive Ethernet Camera

**Solution Today**
Salsa + BroadR-Reach PHY

- LVDS Elimination
- Ethernet proven in mass production

**Integration:**
Reduced PCB FootPrint

- BroadRreach phy integrated through SiP (stacked die wire bond)
- Small low cost package (8x8mm)
- Cost, size, complexity reduction

- MPC5606E integrates the MPC5604E (from Freescale) and the BCM89810 (from Broadcom) dies into a single package
- MPC5606E performance and functionality is equivalent to the dual-chip solution
- Software from dual-chip solution reusable for MPC5606E
- MPC5606E significantly reduces PCB space
  - Ideal for applications (i.e. camera module) that have tight space constraints
  - Package: 8mm x 8mm 121-pin BGA
- Product Availability (from Freescale)
  - Samples: Today  Qualification: June 2014
Freescale Ethernet Camera Software

- **Purple**: AUTOSAR OS 3.0, licensable from Freescale
- **Green**: Camera Application Software, licensable from Freescale
- **Blue**: Ethernet Streaming Software, licensable from Freescale
- **Orange**: Off the shelf Software, licensable from 3rd party (Elektrobit, IXXAT)
- **Red**: Hardware

### Control Algo
Data rate control + buffer overflow protection

### Camera application
- STREAM IF wrapper for a standardized interface
- PTP v2 Stack (IXXAT, optional)
- Normal IP-Stack (Elektrobit)
- AVA_LL_PTP_if (wrapper)
- AVA_LL_EB_if (wrapper+limiter)
- AVA_LL_FEC_DRIVER Ethernet Low level Driver Freescale

### Ethernet MAC
- Ethernet MAC

### Library components:
- Video_encoder
- jpeg_encoder
- I2C HW
- PORT HW
- Imager

### Stack components:
- UDP Stream Builder
- 1722 Stream Builder
- I2C HW PORT
- Sensor interface
- Port PIN initialization, controlling static signals like imager reset
- I2C driver
- ICTR (imager init)
- Control Algo
- Data rate control + buffer overflow protection

### Software components:
- Control Algo
- Data rate control + buffer overflow protection
- STREAM IF wrapper for a standardized interface
- PTP v2 Stack (IXXAT, optional)
- Normal IP-Stack (Elektrobit)
- AVA_LL_PTP_if (wrapper)
- AVA_LL_EB_if (wrapper+limiter)
- AVA_LL_FEC_DRIVER Ethernet Low level Driver Freescale

### License information:
- AUTOSAR OS 3.0, licensable from Freescale
- Camera Application Software, licensable from Freescale
- Ethernet Streaming Software, licensable from Freescale
- Off the shelf Software, licensable from 3rd party (Elektrobit, IXXAT)
- Hardware
i.MX 6 Family

i.MX 6Solo

- Single ARM Cortex A9 at up to 800MHz auto / 1.0GHz consumer
- 256KB L2 cache, Neon, VFPvd16, TrustZone
- 3D graphics with 1 shader up to 27MT/s, plus hardware X-acceleration engine
- External memory support up to 32bit DDR3 and LPDDR2

i.MX 6Dual

- Dual ARM Cortex A9 at 850MHz and 1GHz auto / 1.2GHz consumer
- 1 MB L2 cache, Neon, TrustZone
- 3D graphics with 4 shaders up to 176MT/s and OpenCL Embedded Profile support, plus hardware OpenVG and X-acceleration
- External memory support up to 64-bit DDR3 and 2-channel 32-bit LPDDR2
- Integrated SATA-II

Common Features of the i.MX 6 Series Platform

- Pin compatible ARM Cortex A9 based solutions up to 1GHz per core for automotive and 1.2GHz per core for consumer
- HD 1080p encode and decode
- 3D video playback in high definition
- Integrated IO’s that include HDMI v1.4, MIPI and LVDS display ports, MIPI camera, Gigabit Ethernet, multiple USB 2.0, PCI-Express, dual CAN controllers, MLB150/50/25 support
- Consumer, Industrial and Automotive temperature range qualifications
- SW support: Google Android™, Microsoft Windows® Embedded CE, Linux®, Linaro™, QNX®, GENIVI™

i.MX 6Quad

- Quad ARM Cortex A9 up to 1GHz
- 1 MB L2 cache, Neon, TrustZone
- 3D graphics with 4 shaders up to 176MT/s and OpenCL Embedded Profile support
- OpenVG accelerator for overlays
- External memory support up to 64-bit DDR3 and 2-channel 32-bit LPDDR2
- ≥ 64 bit bus architecture
- Integrated SATA-II
High Bandwidth Networked Automobile

Peripheral Functions and Upgrade Options (Trunk)

- Comm/Telematics
- Audio Amp
- Switch
- Ethernet AVB
- Digital Radio/TV
- NVH Engine
- Ethernet AVB
- USB/IPOD
- Audio out
- NAND flash
- LVDS

Rear Seat Entertainment

- NAND flash
- USB/IPOD
- Audio out
- Display
- LVDS

Infotainment: i.MX

- Media Server/Disc Player

Gateway: Fado, Bolero

- Ethernet AVB
- Multi-Stream Audio/Control
- Service & Control

Switch

- Ethernet
- Multi-Stream Audio/Video
- Ethernet AVB

Cluster: Laser

- Ethernet
- Front-View Camera

Panorama View

Bandwidth + Integration + Low Power

freescale

SAFETY ASSURE
**SCP22xx Image Cognition Processors**

**Smart Camera Technology**

**Balances Performance and Power** –
APEX™ IP offers industry-leading performance per mwatt and delivers an ideal solution for image cognition processing.

**Mainstream Cost-effective Solution** –
Cost, power and size advantages enables smart camera technology into mainstream vehicles, improving auto safety features.

**Delivers the Right Integration** –
Image cognition processor delivers the innovative technology required for smart automotive camera applications.

**Speeds Time to Market** –
Comprehensive solution including libraries, hardware and software development kits speeds time to market.
SCP2201/07 : “Value Add” for Smart Rear Camera

- Dedicated image processor for Distance Measurement and Object detection

- 1st generation array controller (Image Cognition Functionality)
  - Massive Parallelism
  - Revolutionary data movement architecture

- Extra high density Memory (to 64MB)

- Very low power (<300mW typ use case)

- SW enablement to provide:
  - Object Detection
  - Distance Estimation
  - Dynamic Overlay
  - Perspective and Lens Distortion Correction
Monitor (SCP220x) Image Cognition Processors

Key Features:
- Main RISC CPU: ARM926EJ @350 MHz
- 1V Core, 1.8~3.3V IO
- APEX supports 34 billion operations per second (BOPs), or 2 billion MACs per second plus a 2nd slave scalar RISC (350MHz)
- Built-in dedicated overlay engine, rotation, supports alpha-blending and overlay
- Drives TFT LCDs directly
- BT656 sensor interface (YUV, 8/10 bit with separate H/VSync)
- Built in TV encoder/Video DAC (NTSC/PAL)
- Many peripherals integrated
- Multiple package options

http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=SCP2200
# APEX Technology – Massively Parallel

<table>
<thead>
<tr>
<th>Features</th>
<th>Benefits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array Processor Unit (APU)</td>
<td>Scalable and fully-programmable massively parallel SIMD processing core</td>
</tr>
<tr>
<td></td>
<td>96 16-bit processors in APEX-1 (up to <strong>34Billion Ops/sec</strong>)</td>
</tr>
<tr>
<td>Data memory co-located within APU</td>
<td>Minimizes access to off-chip memory to maximize performance efficiency and reduce power</td>
</tr>
<tr>
<td>Multi-channel, Stream-In, and Stream-Out DMAs</td>
<td>Data transfer operations are automatically sequenced to move data in and out of APEX efficiently – keeps APU fed</td>
</tr>
<tr>
<td>Multi-core</td>
<td>Various hardware blocks run in parallel with APU. Bit processing acceleration blocks (not shown) and RISC CPU are used for operations that map best to serial processing.</td>
</tr>
</tbody>
</table>
Vertical Platform Solution

- **PDK**
  - Small form factor
  - Low power dissipation
  - Develop, Prototype, Demonstrate

- **RDK**
  - Reference development kit to support prototype software design & demos

- **SDK**
  - Differentiated libraries & licensable tool kits – patented software algorithms – faster TTM

Software development is a critical cost and factor in time to market
The Road Ahead: Possible, Probable & Plausible

Safety, Security, Data Transportability

Safety with security ⇒
Multiple simpler units within one package
Protected fabrics
Easier configurability and data transport

Development Models

Big data and open standard ⇒
new model for business.
Database, Open SW &
Applications for intelligent
systems enabling Tiers/OEM
to develop in faster and more
creative ways

Technology Trends

Beyond tradition ⇒ Hybrid technology,
packaging
Be first in adoption. Leverage available
technology

Architectural Options

Large clusters and distributed
domains
XXL Computational Performance
Neural networks – flexibility and
adaptability
Power at the service of
Performance

Automotive Networking

Beyond LIN, CAN or FlexRay
⇒ Ethernet as data-robust
highway for ADAS and up-
scalable data distribution
Digitalize and manage network
Designing with Freescale

Tailored live, hands-on training in a city near you

2014 seminar topics include
• QorIQ product family update
• Kinetis K, L, E, V series MCU product training

freescale.com/DwF